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NAME OF INVENTOR: Xian J. Ning
3272 Marcy Street
Mohegan Lake, NY 10547

TITLE OF INVENTION: Vertical MIMCap Manufacturing Method

TO WHOM IT MAY CONCERN, THE FOLLOWING IS
A SPECIFICATION OF THE AFORESAID INVENTION

Vertical MIMCap Manufacturing Method

CROSS-REFERENCE TO RELATED APPLICATIONS

Embodiments of the present invention are related to commonly-assigned U.S. patent applications serial number 09/742,918 filed on December 21, 2000 by Ning, entitled "Self-Aligned Double-sided Vertical MIMCap", and serial number 09/977,004 filed on October 12, 2001 by Ning, entitled "Vertical/Horizontal MIMCap Method", which are incorporated herein by reference.

TECHNICAL FIELD

Embodiments of the present invention relate generally to the fabrication of semiconductor devices, and more particularly to metal-insulator-metal capacitors (MIMCap's).

BACKGROUND

Semiconductor devices are widely used for integrated circuits for electronic applications, including radios, televisions and personal computing devices, as examples. Such integrated circuits typically include multiple transistors fabricated in single crystal silicon. It is common for there to be millions of semiconductor devices on a single semiconductor product. Many integrated circuits now include multiple levels of metallization for interconnections.

The manufacturing process flow for semiconductors is generally referred to in two time periods: front-end-of-line (FEOL) and back-end-of-line (BEOL). Higher temperature processes are typically performed in the FEOL, during which impurity implantation, diffusion and formation of active components such as transistors are performed on a semiconductor substrate of a wafer. Lower temperature processes usually take place in the BEOL,

which is generally considered to begin upon the formation of the first metallization layer on the wafer.

Capacitors are elements used extensively in semiconductor devices for storing an electric charge. Capacitors essentially comprise two conductive plates separated by an insulator. The capacitance, or amount of charge held by the capacitor per applied voltage, is measured in farads and depends upon a number of parameters such as the area of the plates, the distance between the plates, and the dielectric value of the insulator between the plates, as examples. Capacitors are used in filters, in analog-to-digital converters, memory devices, and control applications, and many other types of semiconductor devices.

One type of capacitor is a MIMCap, which is used frequently in mixed signal devices and logic devices, for example. MIMCap's are used to store a charge in a variety of semiconductor devices, such as mixed signal and analog products. MIMCap's typically require a much lower capacitance than deep trench memory capacitors used in dynamic random access memory (DRAM) devices, for example. A MIMCap may have a capacitance requirement of 1 fF/micrometer^2, for example.

Recently, there has been an increase in demand for MIMCap's embedded in BEOL integrated circuits. MIMCap's typically are horizontal MIMCap's comprising two metal plates that sandwich a dielectric parallel to the wafer surface. Prior art horizontal MIMCap's are usually manufactured in the BEOL by forming the bottom capacitive plate in the first or subsequent horizontal metallization layer of a semiconductor wafer. A capacitor dielectric is deposited over the bottom capacitive plate, with a second mask, pattern and etch step being required to form the top capacitive plate.

Alternatively, MIMCap's may be formed between horizontal metallization layers in the BEOL in additional horizontal layers, with each plate requiring a separate pattern and etch level.

A horizontal MIMCap requires a relatively large amount of surface area on a semiconductor wafer. A horizontal MIMCap is a large flat capacitor positioned parallel to the wafer surface covering a large area of the chip, and therefore, MIMCap's do not provide a high area efficiency. As the demand for the capacitance increases, it is desirable to develop MIMCap's that utilize the chip area as efficiently as possible.

A vertical MIMCap, described in patent application serial number 09/742,918 for "Self-Aligned Double-sided Vertical MIMCap", incorporated herein by reference, discloses a vertical MIMCap structure and method that improves the efficiency of the use of chip surface area. Patent application serial number 09/977,004 for "Vertical/Horizontal MIMCap Method", also incorporated herein by reference, describes another way of manufacturing a vertical MIMCap. Vertical MIMCap's are advantageous in that they may be formed in the same inter-level dielectric as metal leads in a metallization layer, saving semiconductor surface area.

SUMMARY OF THE INVENTION

Embodiments of the present invention include novel methods of fabricating vertical MIMCap's. Methods of manufacturing high area efficiency vertical MIMCap's embedded in damascene BEOL metallization layers are described herein, with minimum process complexity added to the common BEOL processes.

In one embodiment, disclosed is a method of fabricating a vertical MIMCap, comprising providing a wafer having a workpiece, depositing an insulating layer

over the workpiece, and patterning the insulating layer with a plurality of trenches. The insulating layer comprises at least one first region and at least one second region, and the first region comprises trenches for at least one MIMCap. The method includes depositing a first conductive layer over the insulating layer within the trenches, depositing a resist over the insulating layer first regions, and depositing a second conductive material within the insulating layer second region trenches. The resist is removed, and a thin dielectric layer is deposited over the insulating layer second region within the second region trenches. A third conductive material is deposited over the thin dielectric layer within the second region trenches.

In another embodiment, disclosed is a method of fabricating a vertical MIMCap, comprising providing a wafer having a workpiece, depositing an inter-level dielectric over the workpiece, and patterning the inter-level dielectric with a plurality of trenches. The inter-level dielectric comprises at least one first region and at least one second region, the first region comprising trenches for at least one MIMCap. The second region comprises trenches for a plurality of conductive lines. The method includes depositing a conductive liner over the inter-level dielectric within the trenches, depositing a seed layer over the conductive liner, and depositing a resist over the conductive liner. The resist is removed over the conductive liner in the inter-level dielectric second regions, leaving resist over the conductive liner in the inter-level dielectric first regions. A first conductive material is deposited within the insulating layer second region trenches to form a plurality of conductive lines, and the resist is removed. A MIMCap dielectric is deposited over the inter-level dielectric second region within the second region

trenches, and a second conductive material is deposited over the MIMCap dielectric within the second region trenches to form a MIMCap top plate.

Advantages of embodiments of the invention include providing a method of fabricating a vertical MIMCap in a BEOL process, where no additional etch steps are required for manufacturing the vertical MIMCap. A single chemical-mechanical polishing (CMP) step is used to form conductive lines and vertical MIMCap's simultaneously. The vertical MIMCap dielectric may be deposited using plasma-enhanced chemical vapor deposition (PECVD). The vertical MIMCap bottom plate may be comprised of a conductive liner and a seed layer. A resist layer is used to mask vertical MIMCap regions while the conductive lines are filled with conductive material.

BRIEF DESCRIPTION OF THE DRAWINGS

The above features of the present invention will be more clearly understood from consideration of the following descriptions in connection with accompanying drawings in which:

Figures 1-6 illustrate cross-sectional views of a semiconductor device including vertical MIMCap's in accordance with embodiments of the present invention, in various stages of fabrication.

Corresponding numerals and symbols in the different figures refer to corresponding parts unless otherwise indicated. The figures are drawn to clearly illustrate the relevant aspects of the preferred embodiments, and are not necessarily drawn to scale.

DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS

Preferred embodiments of the present invention will be described, followed by a discussion of some advantages

of fabricating a vertical MIMCap in accordance with embodiments of the invention.

Figures 1-6 show cross-sectional views of a semiconductor device including vertical MIMCap's in accordance with an embodiment of the present invention, in various stages of fabrication. A semiconductor wafer 10 includes a workpiece 12, shown in Figure 1, which may include a semiconductor substrate comprising silicon or other semiconductor materials covered by an insulating layer, for example. Workpiece 12 may also include other active components or circuits formed in the FEOL, not shown. Workpiece 12 may comprise silicon oxide over single-crystal silicon, for example. The workpiece 12 may include other conductive layers or other semiconductor elements, e.g. transistors, diodes, etc. Compound semiconductors such as GaAs, InP, Si/Ge, SiC, as examples, may be used in place of silicon.

An insulating layer 14 is deposited over the workpiece 12. The insulating layer 14 preferably comprises an inter-level dielectric (ILD) layer, e.g., the wafer first or second inter-level dielectric, as examples, that conductive leads in a metallization layer may also be formed within elsewhere on the wafer 10. The insulating layer 14 preferably comprises silicon dioxide (SiO_2) and may alternatively comprise other dielectric materials such as low dielectric constant materials or high dielectric constant materials, for example.

The insulating layer 14 is patterned and etched, preferably in a damascene process, for example, to form trenches 13/15. The patterning process may comprise a single damascene or dual-damascene process, as examples. In accordance with embodiments of the invention, the insulating layer 14 is preferably lithographically patterned and reactive ion etched (RIE) to form trenches 15 in a first region 19 of insulating layer 14, the first

region 19 comprising areas where vertical MIMCap's will be formed, and trenches 13 in at least one second region 17 where conductive lines or wiring may be formed. The trenches 13/15 may be 0.2 μm wide and 0.4 to 0.6 μm deep, as examples, although the trenches 13/15 may also comprise other dimensions.

A first conductive layer is disposed over the insulating layer 14. First conductive layer includes a conductive liner 16 and a seed layer 18.

The conductive liner 16 is deposited or formed over the insulating layer 14 within the trenches 13/15. The conductive liner preferably comprises a TaN, TiW, Cu, Si, or combinations thereof, as examples, deposited by CVD or physical vapor deposition (PVD), for example.

A seed layer 18 is deposited or formed over the conductive liner 16. Preferably, the seed layer 18 comprises a conductive material comprising, for example, copper, and is deposited by PVD or CVD. In accordance with embodiments of the invention, the conductive liner 16 and seed layer 18 are adapted to improve the deposition of conductive material subsequently deposited in second regions 17. The conductive liner 16 and seed layer 18 also function as a MIMCap bottom plate in first region 19.

A resist 20 is deposited over the entire wafer 10 surface, over the first conductive layer. The resist 20 preferably comprises a photoresist or other type of organic polymer typically utilized as a resist material in the art. The resist 20 does not completely fill the trenches 13/15, but rather, leaves gaps 22 remaining within the bottom of the trenches 13/15.

The wafer 10 is exposed to a lithography process to pattern the resist 20, and the resist 20 is exposed. The resist 20 over second region 17 is removed, leaving trenches 13 in second region 17 exposed, as shown in Figure 3.

A lithography pattern is formed so that the MIMCap regions are opened and other areas blocked by the resist 20. A lithography mask, not shown, may be used to pattern the resist 20 with a predetermined pattern that defines the shape, size and location for at least one vertical/horizontal MIMCap. The wafer 10 is exposed, for example, to a UV light, and developed to remove undesired portions of resist 20 using either a positive or negative exposure process, leaving the structure shown in Figure 3 having resist portions 20 residing over regions 19, leaving regions 17 exposed.

A second conductive material 24 is deposited over the wafer 10, as shown in Figure 4 to form first conductive lines 25 in second regions 17. The second conductive material 24 preferably comprises a metal such as copper, and alternatively, may comprise other conductive materials such as Al, TiN, Ti, W, other conductive materials, or combinations thereof, deposited by PVD or CVD, as examples. The second conductive material 24 may be part of an M1 or M2 metallization layer, for example. The depth of first conductive lines 25 may be the same as other metallization lines of the wafer 10, or the depth of first conductive lines 25 may be the total thickness of a via and wiring line, for example, the total thickness of the first insulating layer 14.

The trenches 15 in the first region 19 of the wafer 10 are blocked by resist 20, and therefore are not covered by the second conductive material 24.

The resist 20 is removed, and a thin dielectric layer 26 is disposed over the wafer 10, covering the second conductive material 24 in the second regions 17, and also covering exposed portions of the seed layer 18 in first regions 19, as shown in Figure 5. The thin dielectric layer 26 is preferably conformal and comprises a thickness in a range of between approximately 10 nm to

200 nm, as an example. Preferably, the dielectric material 26 comprises silicon nitride, Ta_2O_5, or combinations thereof by plasma-enhanced chemical vapor deposition (PECVD) or combinations thereof, deposited by plasma enhanced chemical vapor deposition. Alternatively, the thin dielectric layer 26 may comprise other dielectric materials such as SiC, saline oxide, tetraethoxysilane (TEOS), silicon dioxide, silicon nitride, silicon oxynitride, barium strontium titanate (BST) or other insulators, as examples. Preferably, the thin dielectric layer 26 is relatively thin, e.g., 10 nm to 200 nm thick, and is conformal. Thin dielectric layer 26 functions as a capacitor dielectric 26 of MIMCap's in region 19, e.g., thin dielectric layer 26 comprises the capacitor dielectric between the vertical/horizontal MIMCap plates comprised of conductive liner 16/seed layer 18, e.g., the first conductive layer, and second conductive material 28.

A third conductive material 28 is deposited over the wafer 10, as shown in Figure 5. The third conductive material 28 is deposited over the thin dielectric layer 26 to fill the trenches 15 in the second region 19 of the wafer 10. The third conductive material 28 comprises the top plate of vertical MIMCap's in region 19. The third conductive material 28 preferably comprises W, TiN, Al, Ta, Ti, TaN, TiW, Cu, Si, or combinations thereof deposited by PVD or CVD, as examples. The third conductive material may comprise any conducting material such as a metal, and preferably comprises CVD W or CVD Al. Alternatively, the third conductive material 28 may be formed by plating, for example.

Finally, a chemical-mechanical polish (CMP) process is performed to remove all materials 28/26/24/18/16 from above the top surface of the insulating layer 14 of the wafer 10. For example, the conductive liner 16, seed

layer 18, first conductive material 24, thin dielectric layer 26, and second conductive layer 28 are removed from the top surface of the wafer 10 during the CMP process, as shown in Figure 6.

A plurality of vertical MIMCap's may be formed in the insulating layer 14 first region 19, and at least two of the vertical MIMCap's may be coupled together.

Embodiments of the present invention have been described herein with resist 20 comprising a positive resist. Alternatively, resist 20 may comprise a negative resist 20, for example. Furthermore, although several vertical/horizontal MIMCap's are shown in region 19 of Figure 6, a plurality of other MIMCap's may be formed within a single insulating layer 14.

While cross-sectional views of the present vertical MIMCap are shown in Figures 1 through 6, the MIMCap conductive lines 25 are preferably square or rectangular, and may run lengthwise along the semiconductor wafer 10 by a distance (not shown) according to the capacitance desired. Alternatively, rather than being parallel, the first and second conductive lines 25 may form other shapes such as U-shape, circles or zig-zags, for example.

Embodiments of the present invention provide several advantages over prior art processes for fabricating vertical MIMCap's. Advantages of embodiments of the invention include providing a method of fabricating a vertical MIMCap in a BEOL process, where no additional etch steps are required for manufacturing the vertical MIMCap. A single CMP step is used to form conductive lines 25 and vertical MIMCap's in region 19 simultaneously. The vertical MIMCap dielectric 26 may be deposited using PECVD. The vertical MIMCap bottom plate is comprised of a conductive liner 16 and a seed layer 18. A resist layer 20 is used to mask vertical MIMCap

regions 19 while the conductive lines 25 are filled with second conductive material 24.

While the invention has been described with reference to illustrative embodiments, this description is not intended to be construed in a limiting sense. Various modifications in combinations of the illustrative embodiments, as well as other embodiments of the invention, will be apparent to persons skilled in the art upon reference to the description. In addition, the order of process steps may be rearranged by one of ordinary skill in the art, yet still be within the scope of the present invention. It is therefore intended that the appended claims encompass any such modifications or embodiments. Moreover, the scope of the present application is not intended to be limited to the particular embodiments of the process, machine, manufacture, composition of matter, means, methods and steps described in the specification. Accordingly, the appended claims are intended to include within their scope such processes, machines, manufacture, compositions of matter, means, methods, or steps.